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A Study of Power Consumption Using High-Speed and Low-Power Comparator advanced ADC

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ABSTRACT

Today, the high performance of electronic equipment is dependent on the development of high-speed analog to digital converter (ADC). And, the most common structure of high-speed ADC is Flash ADC. The design of comparator is the most critical part in the Flash ADC, since the speed and the resolution of Flash ADC is determined by the comparator. In this paper, a high-speed low-power comparator, which is used in a 2 Gsps, 8 bit Flash ADC, is designed and simulated. Based on 0.18 um TSMC CMOS process model, the comparator circuit is simulated with a 1.8V power supply in Cadence environment. The result shows that it can work at a 2GHZ clock frequency, and the dynamic power consumption is only 1.2mW, with 123.5ps transmission delay. In addition, the average offset voltage of this comparator is only 676.3uV, which can meet the requirements of an 8-bit Flash ADC.There have three types of comparator can provide the high speed, such as multistage open loop comparator, the dynamic latch comparator, and the preamplifier-latch comparator. The multistageopen loop comparator can meet high-speed and high-precision, but it is hardly can provide the speed more than 1Gsps.The dynamic latch comparator is widely utilized to satisfy the need for high-speed. However, this kind of comparator has large offset voltage which affects the resolution of Flash ADC. The preamplifier-latch comparator can obtain high-speed and high-resolution because of its circuit structure. In this paper, by considering factors of speed and resolution, preamplifier-latch comparator is the choice for Flash ADC.

1. Introduction

Lower power consumption and higher bandwidth are now the two dominant requirements in designing next-generation high-end applications. The global trend across multiple markets is for higher bandwidth in the same footprint at the same or lower power and cost. The Internet is going mobile and video is driving bandwidth requirements at a growth rate of 50% year on year. The march to 40G and 100G systems (with 400G on the horizon) is underway to support this ever-growing bandwidth demand. Fierce competition is driving down prices. Space constraints abound, and cooling solutions often dominate the power budget, sometimes up to twice the power consumption of the electronics. The next generation of 28-nm highend Altera FPGAs addresses these challenges through leading-edge technological innovation, integration, and reduced power consumption.Designing next-generation FPGAs to address the current trend of higher bandwidth and lower power is becoming much more challenging. Many factors must be carefully considered when planning a new FPGA family to ensure the new devices can address the power and performance requirements of the targeted applications in various market segments. These factors include selecting the right process technology, designing the right architecture, applying the right software power optimization, and enabling easier and power-efficient system-level design. Altera took a holistic approach in designing Stratix V FPGAs to deliver the lowest power and highest bandwidth FPGAs in the industry. Key innovations were introduced at various levels to optimize the Stratix V FPGAs' power and performance for designers looking to build a higher bandwidth design while reducing thermal power consumption (Figure 1).

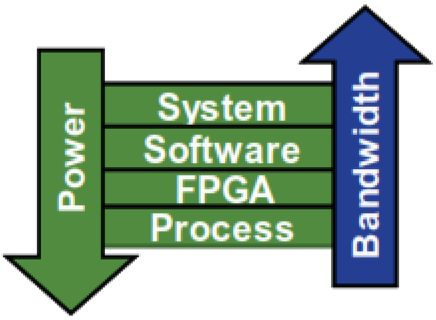


Figure 1. Altera's Holistic Approach to Reduce Power and Increase Bandwidth

2. Power Consumption In High-End FPGA Designs

There are three components to power consumption: static, dynamic, and I/O power.

Static Power

Static power is the power consumed by the FPGA when no signals are toggling. Both digital and analog logic consume static power. The sources of static leakage current in 28-nm transistors are shown in Figure 2 and Table 1.

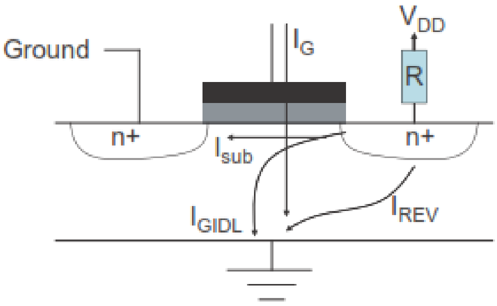


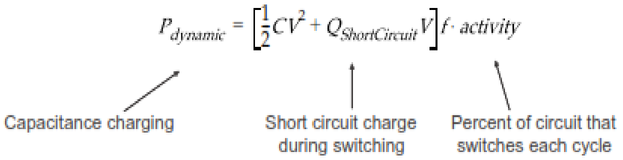
Figure 2. Sources of Transistor Leakage

Table 1. Main Sources of Transistor Leakage

Main Sources of Leakage	**Impact**	**Mitigation Techniques**
Subthreshold leakage (I_{sub})	Dominant	■ Lower voltage ■ Higher voltage threshold ■ Longer gate length ■ Dopant profile optimization
Gate direct-tunneling leakage (I_G)	Dominant	High-k metal gate (HKMG)
Gate-induced gate leakage (I_{GIDL})	Small	Dopant profile optimization
Reverse-biased junction leakage current (I_{REV})	Negligible	Dopant profile optimization

Dynamic Power

Dynamic power is the additional power consumed through the operation of the device caused by signals toggling and capacitive loads charging and discharging. As shown in Figure 3, the main variables affecting dynamic power are capacitance charging, the supply voltage, and the clock frequency. Dynamic power decreases with Moore's law by taking advantage of process shrinks to reduce capacitance and voltage. The challenge is that as geometries shrink with each process shrink, the maximum clock frequency increases. While the power reduction declines for an equivalent circuit from process node to process node, the FPGA capacity doubles and the maximum clock frequency increases.



$$P_{dynamic} = \left[\frac{1}{2}CV^2 + Q_{ShortCircuit}V\right] f \cdot activity$$

Figure 3. Variables Affecting Dynamic Power

I/O Power

I/O power includes the power consumption consumed by I/O blocks, including general-purpose I/Os and high-speed serial transceivers. The main factors impacting general-purpose I/O power consumption are shown in Figure 4 and summarized in Table 2.

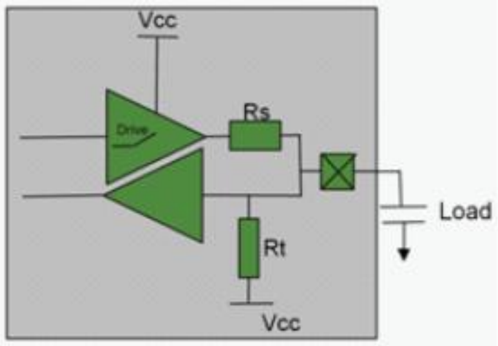


Figure 4. Factors Impacting General-Purpose I/O Power

Table 2. Main Factors Impacting General-Purpose I/O Power

Main Factors Impacting I/O Power	**Mitigation Techniques**
Termination resistors (on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT))	Dynamic on-chip termination (DOCT)
Output buffer drive strength	Programmable drive strength
Output buffer slew rate	Programmable slew rate
I/O standard (single ended, voltage referenced, or differential)	Support for multiple I/O standards
Voltage supply	Support for various voltage rails
Capacitive load (charging/discharging)	Interface dependent

The main factors impacting the power consumption of high-speed serial transceivers include:

- Data rates (Gbps)
- Pre-emphasis and equalization settings
- Interface load (chip-to-chip or chip-to-backplane)
- Transceiver circuit design

Figure 5 shows the breakdown of total power across various high-end FPGA customer designs. Dynamic and I/O power dominate the FPGA's total power consumption. Because high-end FPGA designs tend to push the envelope in terms of bandwidth and performance, they use more logic running at a higher clock fMAX. With I/Os toggling at higher data rates and logic toggling at faster frequencies, the charging and discharging of loads on and off chip becomes the main consumer of FPGA power. To effectively reduce total FPGA power, both static and dynamic power must be addressed while ensuring the FPGA's performance still meets design requirements.

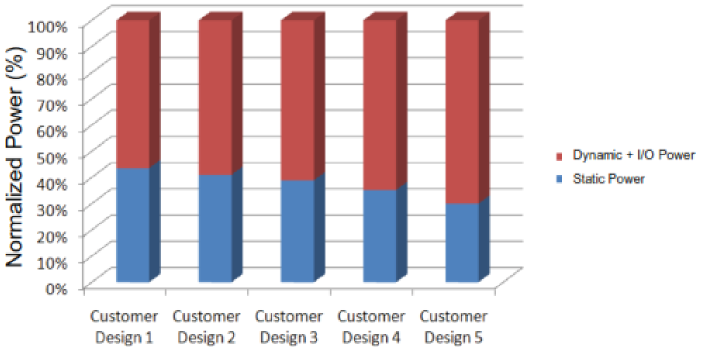


Figure 5. Total Power Breakdown across Various High-End FPGA Customer Designs

3. Structure of Preamplifier-Latch Comparator

A comparator, by definition is 'a circuit that compares the two analog input signals and decodes the difference into a single digital output signal' [4].The preamplifier-latch comparator is consisting of preamplifier, regenerative latch comparator and an output latch. The preamplifier's role is to amplify input analog signals. Then, the regenerative latch comparator compares the enlarged signals from the preamplifier. As the last stage, output latch deals with the results from the regenerative latch comparator, and generates the digital level (1 or 0) as the final output of comparator. In the preamplifier-latch comparator, the main roles of preamplifier: firstly, it can amplify the input signals to reduce the comparison time of regenerative latch comparator so as to improve the speed of comparator; in addition, it also can amplify the differential input signals to reduce the influence of the offset voltage. Therefore, the preamplifier should have a high gain and a wide bandwidth. In general, in order to improve the speed of comparator, the first choice for latch comparator is regenerative loop structure [5]. The regenerative latch compared input signals by a positive feedback. It can quickly amplified input signals to improve the speed [6]. In order to have a stable digital level, it is better to add an output latch after the regenerative latch comparator. So output latch is the last stage of comparator, and the final output will be generated by it [7]. When the regenerative latch comparator is in the reset mode, output latch will keep the level of the last clock period. Output latch will generate the final output when the regenerative latch comparator is in the compare mode.

The overall schematic of the high-speed and low-power comparator is shown in Fig 6.

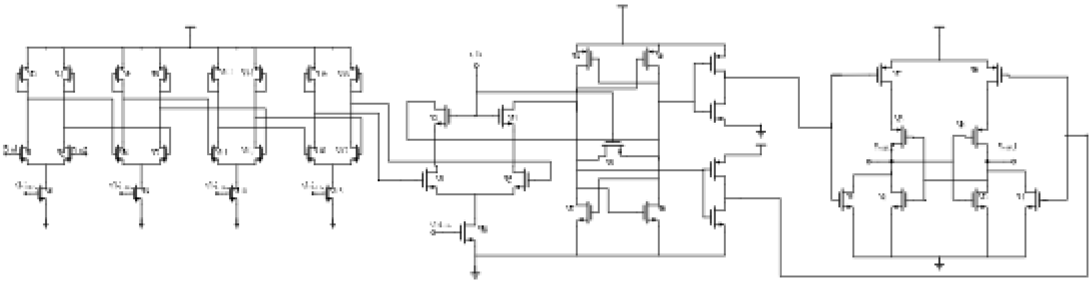


Fig. 6 The Overall Comparator circuit

4. Optimization of Comparator

1. Optimization of Preamplifier

To get high bandwidth and high gain, the preamplifier needs multistage amplifiers. But with the increase of stages, the transmission delay will increase, and the offset voltage also increases. Meanwhile,the layout area and power consumption increase. Therefore, it is very important to select the number of stages to reduce the delay of preamplifier. The delay of preamplifier can be expressed by equation (1):

$$t = n\tau = \frac{n \cdot A^{\frac{1}{n}}}{G \cdot BW} = \frac{1}{G \cdot BW} \cdot n \cdot A^{\frac{1}{n}} \tag{1}$$

Where, t is the delay of preamplifier, n is the number of amplifiers, r is the delay of each amplifier, A is the gain of preamplifier, G is the gain of each amplifier; BW is the bandwidth of each amplifier. Fig 7 shows the simulation results of equation (1) with Matlab software tools. In Fig 8, X axis describes the number of amplifiers n, Y axis expresses total gain A, Z axis shows the transmission delay of preamplifier t. For the minimum of transmission delay, n is best to be 2, 3 or 4. What's more, the preamplifier must have enough gain to amplify the input signals and to reduce the offset voltage of comparator. Considering factors of gain and transmission delay, the preamplifier should be consisting of 4 stages of amplifier whose gain is about constant e.

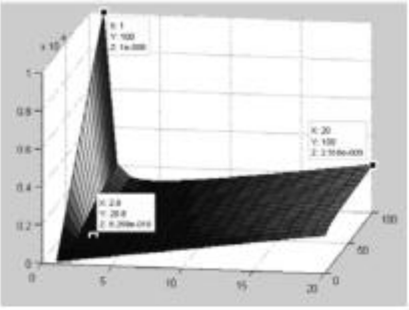


Fig. 7 Simulation Results of Equation (1);

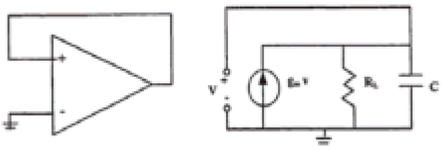


Fig. 8 The small signal model

2. Reduce the delay of Regenerative Latch Comparator

The regenerative latch comparator uses the positive feedback and amplifier to realize the comparison of two input signals. As shown in Fig 8, the small signal model of regenerative latch comparator is from an amplifier with positive feedback [8]. According to the small signal model, the transmission delay can be analyzed as follows:

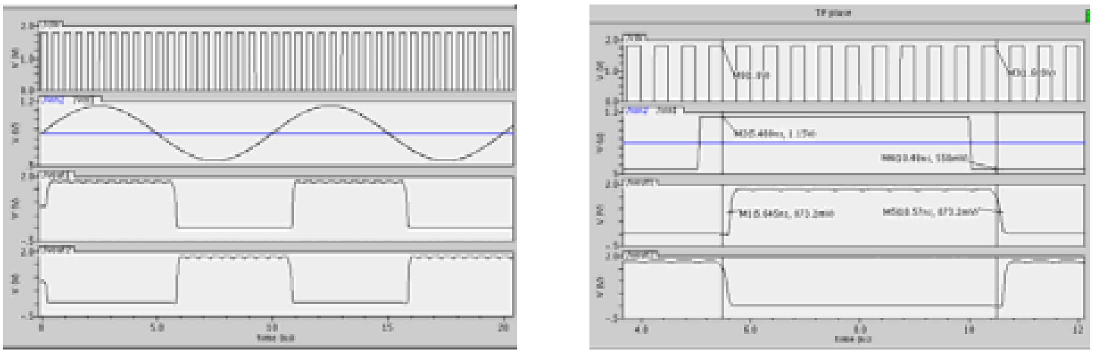
$$g_m V = \frac{V}{R_L} + C\frac{dV}{dt} \qquad (2)$$

Where, C is the total capacitance, including input capacitance and output capacitance. From the integration of equation (2), the transmission delay time is as follows:

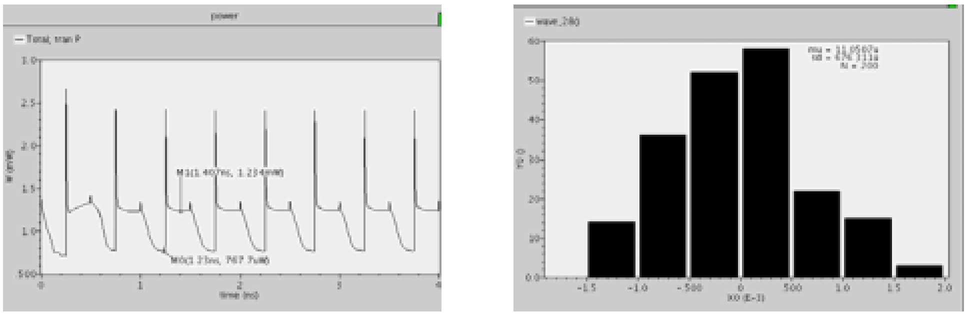
$$\Delta t = t_2 - t_1 = \ln\left(\frac{V_2}{V_1}\right)\cdot\frac{C}{g_m}\left(1+\frac{1}{g_m R_L - 1}\right) \qquad (3)$$

5. Simulation Results

Based on TSMC 0.18um CMOS process model, the high-speed and low-power comparator is simulated with Spectre of Cadence. The comparator's clock frequency is 2GHZ, and the voltage of power supply is 1.8V. Firstly, there is the logic simulation result of the preamplifier-latch comparator in Fig 9 (a) .When vin1 is bigger than vin2, the output terminal vout1 is at high level, and vout2 is at low level. Secondly, the transmission delay of comparator is shown in Fig 9 (b). It is seen that the transmission delay between input and output signals is about 123.5ps. The small delay can make the comparator work normally under the high-frequency clock. Thirdly, the power consumption of comparator is simulated, as shown in Fig 9 (c). When the regenerative latch is in the reset mode, the static power consumption of the whole comparator is only 767.7uW. But when the regenerative latch is in the compare mode, the dynamic power consumption of the whole comparator is about 1.234mW. Therefore, the average power consumption is about 1mW. And then, the comparator is simulated for 200 times Monte Carlo, and the offset voltage simulation result is shown in Fig 9 (d). The offset voltage distributes between -1.5 mV and + 2 mV, and the average offset voltage is only 676.3uV.



(a) logic simulation of comparator; (b) transmission delay of comparator



(c) power consumption of comparator; (d) offset voltage of comparator

Fig. 9 Simulation Results

6. Conclusion

This paper proposed a high-speed and low-power comparator in Flash ADC. Due to increase the speed of the comparator, this paper optimizes the preamplifier and the regenerative latch comparator. The results show that it can work at a 2GHZ clock rate, and the transmission delay time is only 123.5ps. What's more, the average power consumption of this comparator is about 1mW.The comparator can be used in Flash ADC because that the average offset voltage of the comparator is only 676.3uV.

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