RESEARCH REVIEW JOURNALS
Volume-04
Issue-02
February -2019

ISSN: 2455-3085 (Online)
RESEARCH REVIEW International Journal of Multidisciplinary
www.rrjournals.com [UGC Listed Journal]

Viterbi Decoder Implementation Using VHDL for Convolution Encoding

[*1]Sreekaram Jagadeesh, [2]D Y Pushpamithra [3] Revanth Kumar T R

[*1]*Assistant Professor, SITAMS (autonomous), jntua university (India)*
[2] *Assistant Professor, SITAMS (autonomous), jntua university (India)*
[3] *Associate Professor, SVEW, jntua university (India)*

ARTICLE DETAILS

Article History
Published Online: 10 February 2019

Keywords
Viterbi Algorithm, Convolution codes, Adaptive Viterbi decoder, Memory path, Register Exchange

[*]**Corresponding Author**
Email: sreekaramjagadeesh[at]gmail.com

ABSTRACT

In modern communication channels in order to improve the capacity of the particular communicating systems Viterbi decoding technique is used as key source in wireless communication domain. In this system for detecting the error and correcting the same error we use comparator in Viterbi decoder. We generally use Viterbi decoder for forward error correction with the combination of convolutional encoding technique, Which is the powerful method to the capacity of the system. For convolution coding most widely used algorithm is Viterbi algorithm which is dynamic to observe the hidden states of the path involved. In this paper, Viterbi decoder is implemented in Xilinx tool and code developed in VHDL. Code executed and simulated using Xilinx ISE and ISIM software and power analysis calculated.

1. Introduction

In digital communication, speed is one of the constraints which is been concentrated these days. First priority is given to the system with high speed for on improving the capacity of the system there has increased interest in high speed Viterbi decoder design. The order of the output is in Giga-bit per second, which is possible with Viterbi decoder using Electronic Design Automatic (EDA) tools without using off-chip processor or memory. The main motive of this paper is to use VHDL for implementing Viterbi decoder which is having the constraint length of 11.

For convolution codes, asymptotically optimal decoding algorithm is developed by Viterbi algorithm, normally which is used for decoding block codes. The advantage of Viterbi algorithm is fixed decoding time which is well suited for implementing hardware decoding. The convolution codes of Viterbi decoder are efficient and robust which requires O (2 n-k) words of memory, where n represents the length of the code and k represents the length of the message, so n-k represents the number of appended parity bits. Practically, code section is done which gives the priority to the highest minimum hamming distance which decodes within the specified time and increased minimum hamming distance implies an increase in number of parity bits. Memory is distributed evenly among the processing elements in Viterbi decoder. [1-3].

2. Convolution Design

2.1. Encoding Process

Commonly we use two parameters to describe convolutional code i.e., the code rate and the constraint length. Code rate is expressed in the form of k/n and the ratio is termed as convolution encoder (k) to the number of channel symbols output in the encoder cycle. k is represented as the constraint length that denotes the length of the convolutional encoder. In practical communication systems, convolutional codes are used for error correction. Decoding strategy for convolutional code is based on widely used algorithm call Viterbi. To encode the data in convolutional way, which starts with memory registers k each will be holding 1 input bit and the value initiates from value 0.The input is given to left most first register which uses generator polynomials [3-5] and remaining registers will use existing values. Bit will shift to next register based on the operation respectively. If there are no input bits left all the register values must return to the value zero.

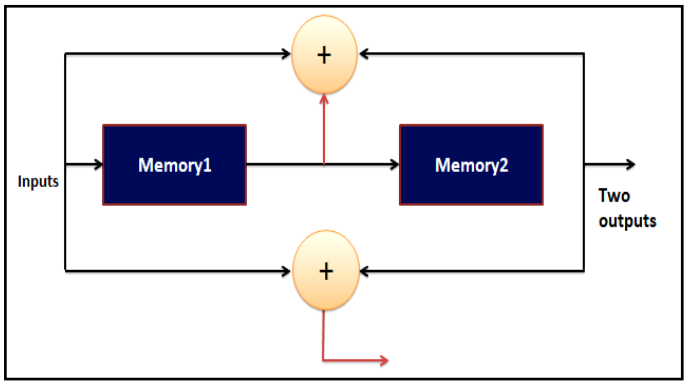


Fig .1. Convolution Encoder ½ rate

2.2. Viterbi Algorithm Design

Decoding of convolutional codes with memory less noise is proposed by A.J.Viterbi. The Viterbi algorithm is a dynamic algorithm which will trace the hidden states signal and perform the error correction and prediction in every state. For convolution coding Viterbi algorithm is the maximum likely-hood decoding algorithm. In practical, maximum likely-hood decoding of codes is done which haves highest minimum hamming distance decodes in specified time and increased minimum hamming distance implies increase in number of parity bits. Memory is distributed evenly among the processing elements in Viterbi decoder. Through trellis most likely path will maximize the metric. To reduce its complexity Viterbi algorithm performs maximum likely-hood decoding. [6-8]. It will be eliminating the paths which are having least likely trellis path.

To reduce the complexity of the system at each stage it will be terminating the unlike paths in the transmission stage. It will get the efficiency by concentrating on the available paths on trellis. When a set of noisy observations are given to the final state for estimating the state of sequence this process is also called as optimum algorithm. Viterbi algorithm implementation consists of three parts namely branch metric computation, path metric updating and survivor sequence generation. To calculate the branch metric which is used to calculate the distance every symbol in the code branch metric computation is used. The output of branch metric computation is given as an input to path metric updating and the output of path metric updating is given as an input to survivor sequence generation. In path metric is used to select the best path in the available paths. Reduction in the complexity of the system results in the improvement of the system speed and capacity. Drawback of the Viterbi decoders is they are very expensive.[7].

3. Viterbi Decoding Section

To encode the bit stream forward error correction technique is been used, Viterbi algorithm is used for Viterbi decoder for encoding the bit stream. There are different algorithms for decoding the conventional encoded stream, among them Viterbi algorithm is one of the resource consuming technique which performs maximum likelihood decoding technique. The following block diagram represents Viterbi decoder which is composed with branch metrics, ACS, register exchange; maximum path metric selection and output register selection.

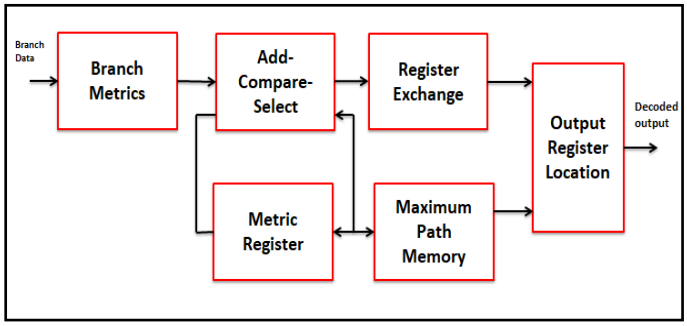


Fig.2. Functional Block Diagram of Viterbi decoder

3.1. Branch Metrics

Branch metrics is one of the building blocks of the Viterbi decoder. Branch metrics performs the comparison of both codes i.e., at the receiver end and the expected code based upon the difference it will calculate the count of the differed bits involved in the code which is given at the input of the decoder. The following diagram represents the block diagram of the branch metrics

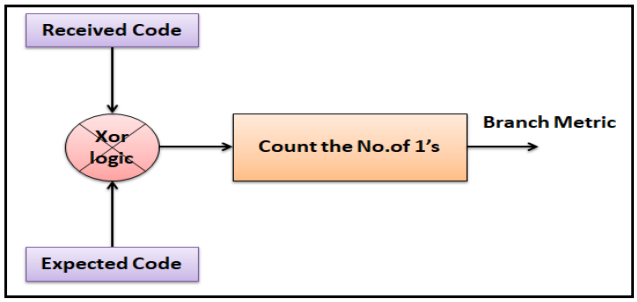


Fig 3. Branch Metrics of Viterbi decoder

Two adders are the building blocks of the branch metrics which will compute the partial path metric involved in every branch and here each branch will be having a comparator which will compare the metrics based upon the comparison the selector is available to select the appropriate branch. Here new partial branch will update the new state metric means the branch which is having no delay compared with other branches survivor path recording is available for recording the available paths.

3.2. Path Metric Calculation and Storage

Path Metric Calculation and Storage is one of the computational unit of Viterbi decoder. In this Path Metric Unit (PMU) the central element is ACS (Add-Compare-Select) circuit which is composed of adder, comparator, selector and several registers in order to calculate the path metric of the each convolutional code state which is the output of the branch metric block. Convolution encoder will be having 'N' number of states which will generate 'n' number of bits each with a constraint length of k and input bits b.Path metric will calculate each and every state, but the actual decision of states is based upon the Viterbi which is trace back operation to find out the states in each and every path. The main characteristic of Viterbi decoder is maximum likelihood path which will cover all the stages at somewhere previous in time.[8-12].

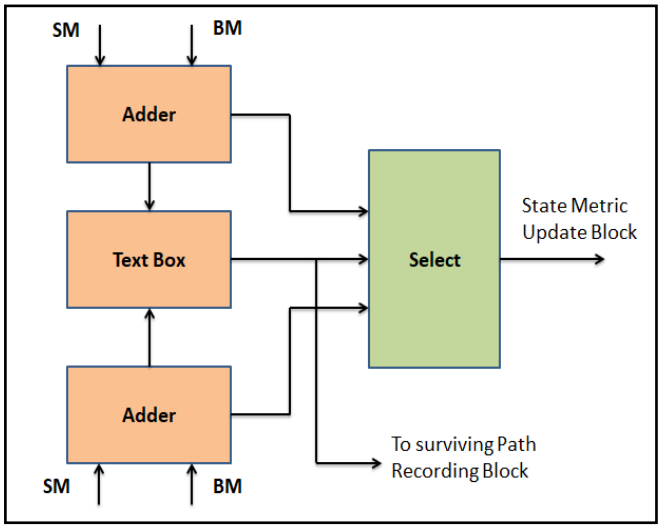


Fig 4. Add-Compare-Select Circuit

3.3. Register-Exchange and Trace Back

Viterbi decoder uses register-exchange approach which will assign the registers to each and every state. Register operation in each state is to record all the outputs from initial stage to final stage. By doing so this approach will eliminate trace back unit, as the final stage output of the register contains high speed operation, but there is a drawback of using this approach as the register need to copy all the data in every stage. Coming to the other approach called trace back approach which trace back all the paths of each and every stage outputs which is known. Here in this approach flip-flop is assigned to store the survivor and existing branches.

3.3.1. Trace back read (tb)

Operations involved in trace back(TB) is of 3 different types, among them one is two read operations which consist of

reading a bit and explain the bit which are present in present state number and previous state number.

3.3.2. Decode Read (dc)

The operation of the decode read is same as trace back unit but in a reversal manner. Trace back unit will operate on the newly generated paths but here decode read will operate on the older data in the memory bank which are given as input to the decode read pointer values i.e., the output of the dc is given as the input to the bit order reversing circuit.

3.3.3. Writing New Data (wr)

In Viterbi decoder, the main function is to the capacity of the systems. So we have used ACS circuit for comparing the signal codes in the system and select the path which is having more accuracy and eliminate the other paths which are having more delay so that the complexity of the system will be reduced. This process is called writing new data.

3.3.4. Selective update and Shift update

Registers can also be implemented using flip-flops by arranging them in vertical direction and horizontal direction. When the flip-flops are placed in vertical direction then it is called selective update. When the flip-flops are placed in horizontal direction then it is called as shift update. When the operation of the register is from left to right it is called selective update. When the existing path is applied to the least significant of all the registers it is called shift update. Here in shift update all the information in the existing path is given from the least significant bit toward the most significant bit.

3.3.5. Survivor path memory

Survivor path memory is as best approach for high speed constrain which improves the capacity of the system. To implement this we have designed an architecture which is composed of 3 building blocks namely Register-Exchange (RE), Trace-Back (TB) and RE-TB combined. For fast decoder operations RE is the best approach but it requires large area and consumes more power's approach uses less memory but slower in operation than RE in order to increase the speed we need to implement the clock in RE which in turn increases the complexity. The combine operation RE-TB which is best alternative for RE approach for high speed applications which improvises the capacity of the system too.[13-16].

4. Results -Viterbi Decoder Implementation using VHDL

Viterbi decoder implemented and tested the performance using Xilinx ISE Package software, here we used VHDL Language. The internal structure of the Viterbi decoder shown in Fig. 5B. For in-depth analysis of the implementation each and every component extraction is required. For that analysis need to extract the block level structure to technical schematic level. Fig 5 C represents the technical schematic level diagram.

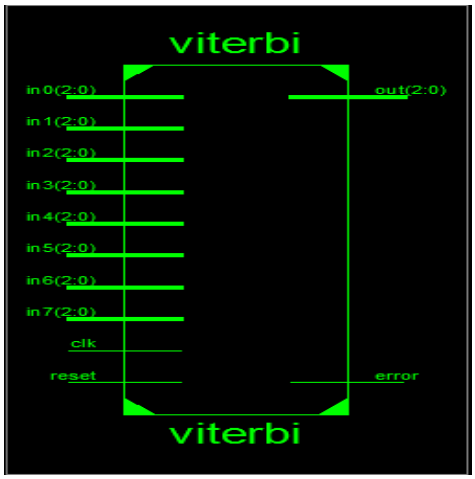


Fig. 5A. Viterbi Decoder implementation in Xilinx using VHDL

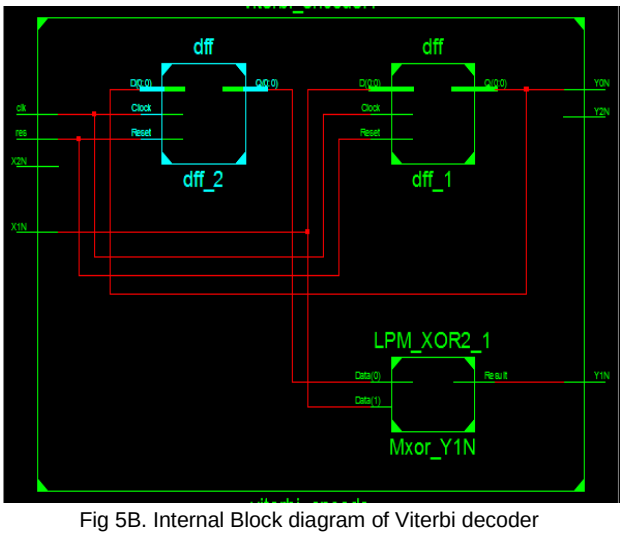


Fig 5B. Internal Block diagram of Viterbi decoder

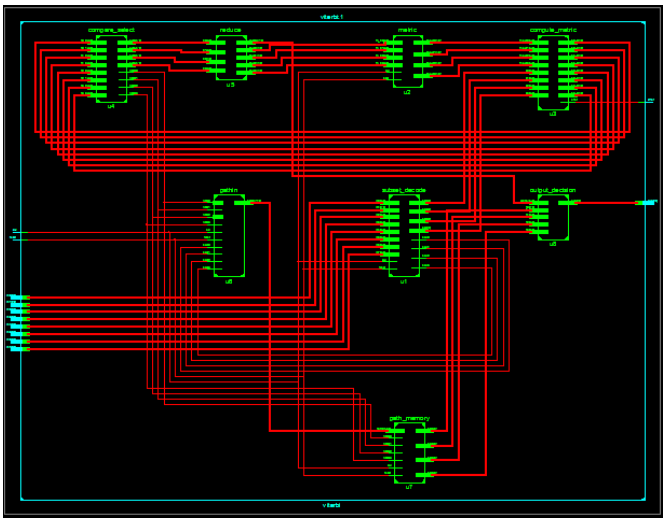
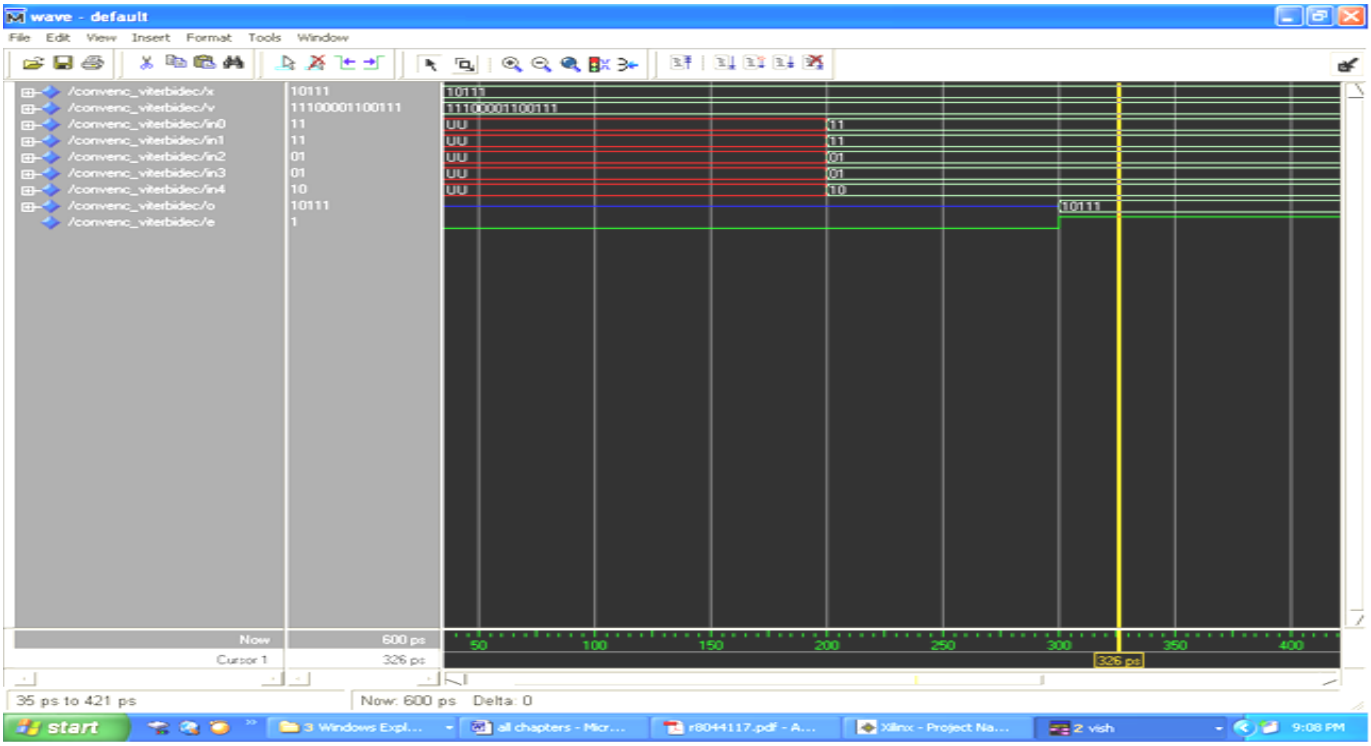


Fig 5C. Internal schematic of Viterbi decoder



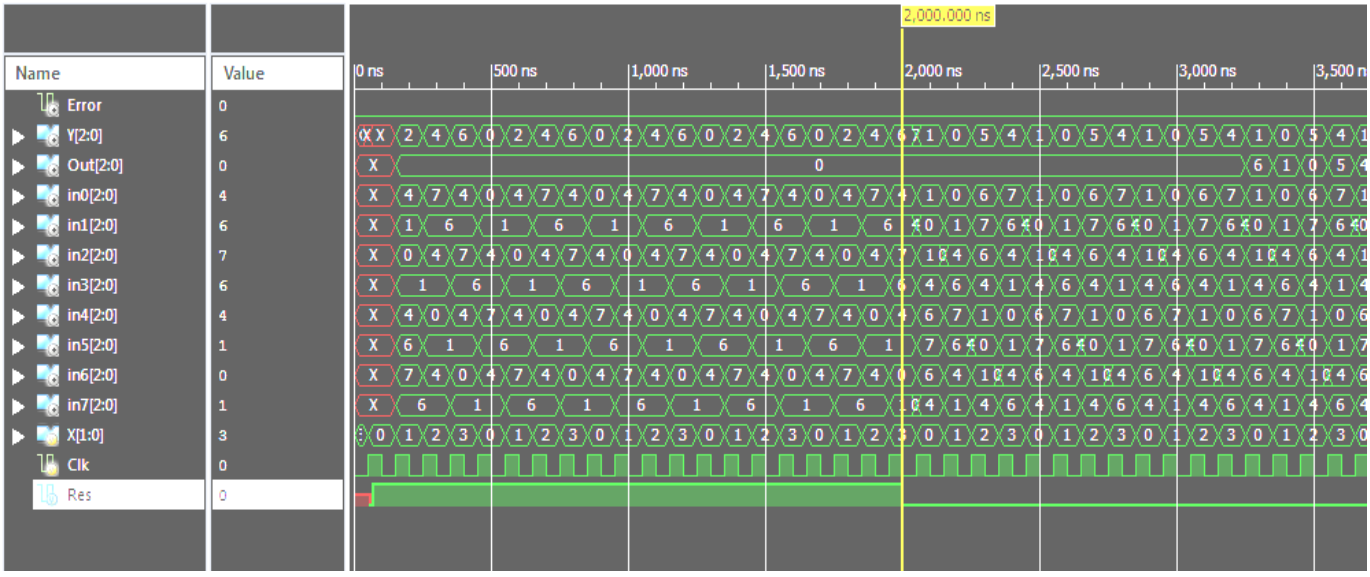


Fig 6 A, B Simulated result- Viterbi decoding process

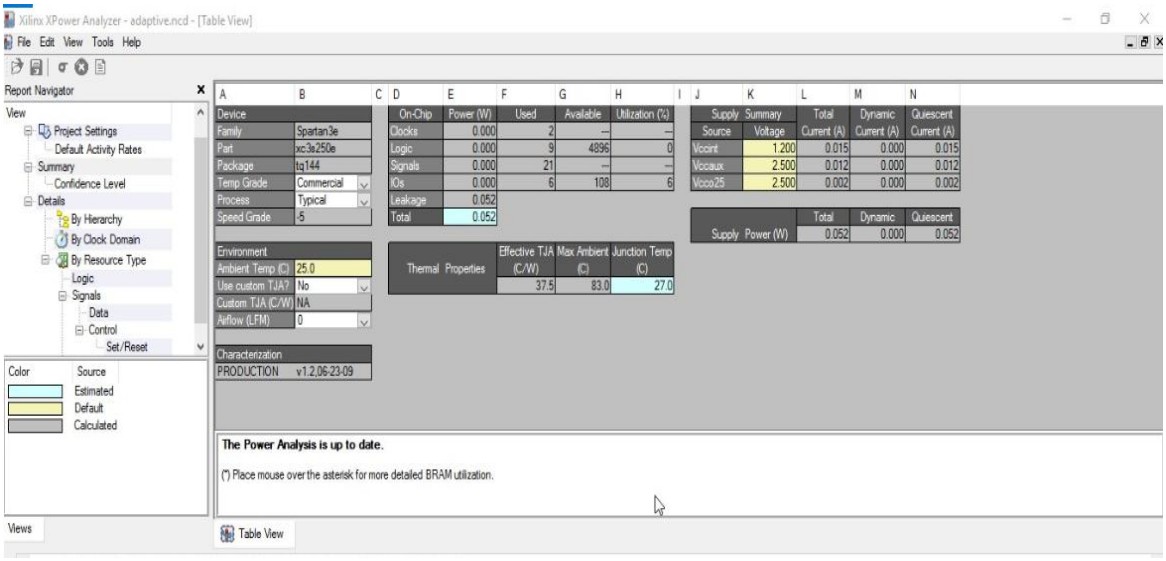


Fig 7. Power Analysis Report

After extracting the technical schematic of the circuit, checking the components connectivity with Vcc and Gnd logics is the important parameters. In order to verify the logic functionality need to execute the simulation. In simulation based on the code logic the output will be achieved. Simulation output shown in Fig 6 A, B.

The decoding logic executed with Viterbi logic, itself it is detecting the path metrics and branch metrics in order to send the data in quick sessions. This concept will be useful communication devices. Power analysis shown in Fig 7. Low power Viterbi decoder designed.

5. Conclusion

In this paper, Viterbi decoder implemented using VHDL coding and analyzed the performance using ISIM Xilinx simulator. Viterbi decoder used in many communication domains especially in wireless domain. So far, using VLSI level implementation Viterbi decoders are performing well, in addition to this concept, real time scenarios observation is required. Viterbi decoder for convolution encoding techniques designed and optimized with subunits. VLSI implementation on CMOS level depends on physical design properties.

References

1. Digital Communication-Simon Hykins, John Wiley & sons Pte Ltd
2. J. Viterbi, "Error bounds for convolutional coding and an asymptotically optimum decoding algorithm", [3] M. S. Ryan, G. R. Nudd, “The Viterbi Algorithm” Warwick Research Report RR238, February 1993.
3. Chip fleming,”A tutorial on Convolutional coding with viterbi decoding”
4. San Ling and Chaoping Xing, “Coding Theory – A first Course”, Cambridge University Press, 2004.
5. Irfan Habib, Özgün Paker, Sergei Sawitzki, “Design Space Exploration of Hard-Decision Viterbi Decoding: Algorithm and VLSI Implementation” IEEE Tran. On Very Large Scale Integration (VLSI) Systems, Vol. 18, Pp. 794-807,May 2010
6. V.Kavinilavu1, S. Salivahanan, V. S. Kanchana Bhaaskaran2, Samiappa Sakthikumaran, B. Brindha and C. Vinoth, “ Implementation of Convolutional
7. Shinghal, R. and Godfried T. Toussaint, "Experiments in text recognition with the modified Viterbi algorithm," IEEE Transactions on Pattern Analysis and Machine Intelligence, Vol. PAMI-l, April 1979, pp. 184–193.
8. 29 Apr 2005, G. David Forney Jr: The Viterbi Algorithm: A Personal History
9. Forney GD (March 1973). "The Viterbi algorithm". Proceedings of the IEEE. 61 (3): 268–278. doi:10.1109/PROC.1973.9030. Subscription required.
10. Encoder and Viterbi Decoder using Verilog Hdl” in IEEE tran. On inform theory, 2011.
11. Samirkumar Ranpara,”On a Viterbi decoder design for low power dissipation,” toward his master’s thesis submitted to virginia polytechnic institute and state university.
12. Ming-Bo Lin, “New path history management circuits for viterbi decoders,” in IEEE transactions on communications, vol 48, no.10, october 2000.
13. Hema.S, Suresh Babu.V and Ramesh.P, “FPGA Implementation of Viterbi decoder” proceedings of the 6th WSEAS ICEHWOC,Feb. 2007..
14. Wong, Y.S. et.al “Implementation of convolutional encoder and Viterbi decoder using VHDL” IEEE Tran. on Inform. Theory, Pp. 22-25, Nov. 2009.
15. S.Lin and D.J. Costello, Error control coding. Englewood cliffs, nj: prentice hall, 1982.
16. Digital Communication-Bernand Sklar, Pearson ducation. [10] Error Control Coding –Oxford Press, New York.

